GERMAN-MALAYSIAN INSTITUTE
Training for Advanced Technology

COURSE TITLE : HARDWARE DESCRIPTION LANGUAGE (VERILOG) BASED SYSTEM DESIGN & APPLICATION

COURSE OVERVIEW

The course is ideal for those who want to understand and acquire knowledge in modeling of digital systems at various levels of abstraction with state-of-the-art hardware description languages (HDLs). Introduction to modern HDLs. HDL-based design methodology. HDL-based modeling of digital systems at behavioral-level, structural-level, RTL-level and gate-level. HDL-based synthesis, simulation and verification of digital circuits. This is a project-oriented course.

COURSE OBJECTIVES

After completing this comprehensive training, you will have the necessary skills to:

- Write RTL Verilog code for synthesis
- Write Verilog test fixtures for simulation
- Create a Finite State Machine (FSM) by using Verilog
- Target and optimize ALTERA FPGAs by using Verilog
- Use enhanced Verilog file I/O capability
- Download to the FPGA demo board

THE UNIQUENESS OF THIS COURSE

- 60% of the course will be practical
- Didactic equipment s that are designed to assist participants in understanding theories

WHO SHOULD ATTEND

This course is designed to those who want to provide student, or engineer with a working knowledge required to describe digital system designs in HDL at behavioral, register transfer, and structural (gate) levels; to validate and/or to verify through simulation, and to synthesize their designs to various target technologies.

TARGET GROUP

Software programmer, Electrical & Electronic Engineers, technicians and technical teachers.

KEY TOPICS

- Verilog Language Concepts
- Building Hierarchy
- Verilog Simulation and RTL Verification
- Timing Simulation
- Implement and Download

METHODOLOGY

Lectures, discussions, Exercises & Practical, Lab work

COURSE DURATION

4 Days / 32 Hours

PRE-REQUISITE

Digital System

CERTIFICATION

Certificate of attendance will be issued to those who fulfill 80% of attendance.

Minimum participants: 3

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SystemVerilog